XT1S112 手册

Ver-1.1

General Description

The XT1S112 is a modular, high performance, low additive jitter, low skew, general-purpose clock buffer. The entire family is designed with a modular approach in mind. All of the devices are pin compatible to each other for easy handling.

The XT1S112 supports an asynchronous output enable control (1G) which switches the outputs into a low state when 1G is low.

The XT1S112 family operates in a 1.8-V, 2.5-V and 3.3-V environment and are characterized for operation from – 40° C to 85° C.

Features

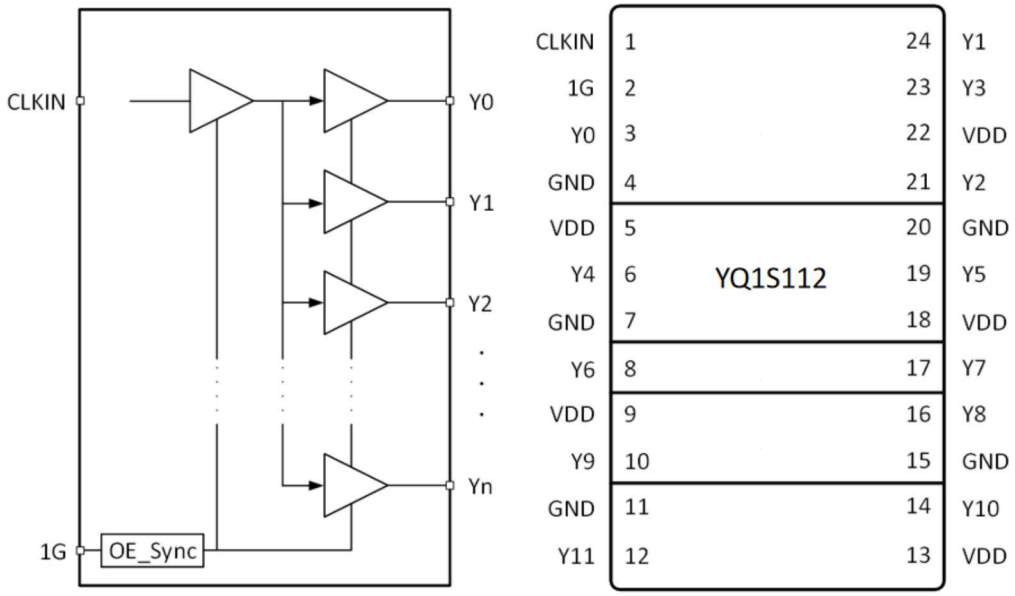
- High performance 12 output channel LVCMOS Clock Buffer
- Very low pin-to-Pin Skew < 50 ps
- Very low additive jitter < 50 fs
- Supply voltage: 1.8-V, 2.5-V or 3.3-V
- Fmax = 250 MHz for 3.3-V

  Fmax = 200 MHz for 2.5-V/1.8-V
- Operating Temperature Range: –40° C to 85° C
- Package: 24-Pin TSSOP

Applications

- General-Purpose Communication
- Industrial,
- Consumer Applications

Block Diagram & Pin Configuration：



Pin Descriptions：

Number	Name	Type	Description
1	CLKIN	Input	Input Clock Pin
2	1G	Input	Clock Output Enable with internal 50-kΩ (typical) pulldown resistor to GND. Typically connected to VDD with external pullup resistor. HIGH: outputs enabled LOW: outputs disabled
3	Y0	Output	LVCMOS output.
4	GND	Ground	Ground
5	VDD	Power	Supply Voltage: 1.8-V, 2.5-V or 3.3-V
6	Y4	Output	LVCMOS output.
7	GND	Ground	Ground
8	Y6	Output	LVCMOS output.
9	VDD	Power	Supply Voltage: 1.8-V, 2.5-V or 3.3-V
10	Y9	Output	LVCMOS output.
11	GND	Ground	Ground
12	Y11	Output	LVCMOS output.
13	VDD	Power	Supply Voltage: 1.8-V, 2.5-V or 3.3-V
14	Y10	Output	LVCMOS output.
15	GND	Ground	Ground

16	Y8	Output	LVCMOS output.
17	Y7	Output	LVCMOS output.
18	VDD	Power	Supply Voltage: 1.8-V, 2.5-V or 3.3-V
19	Y5	Output	LVCMOS output.
20	GND	Ground	Ground
21	Y2	Output	LVCMOS output.
22	VDD	Power	Supply Voltage: 1.8-V, 2.5-V or 3.3-V
23	Y3	Output	LVCMOS output.
24	Y1	Output	LVCMOS output.